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Chip Assembly on MID (Molded Interconnect Device) – A Path to Chip Modules with increased Functionality

The MID (Molded Interconnect Device) technology enables the production of non-planar chip assembly substrates. In addition to their multidimensional chip carrier function, they can also provide additional functions, and directly represent a part of the housing or connector, for example. Based on the techniques for planar substrates, we are now developing chip assembly processes on those specially shaped plastic carriers, in order to realize chip assemblies on MID on an industrial scale, serving a wide field of applications. These technologies allow e.g. the realization of application specific, compact sensor modules which fix the sensing element in a suitable location and include simultaneously all connections and interfaces to the system.

MIDs

Molded Interconnect Devices (MIDs) are injection molded plastic elements carrying electrical lines, and thereby represent a kind of 3D PCB. Their electrical connections may be routed “around corners”, while components may be mounted in various spatial directions. In addition to this space-saving feature, the injection molding enables the creation of additional functions, such as the direct integration of the element into the housing, or the direct implementation of special geometrical shapes such as recesses, channels and openings for measuring sensors, as well as the possibility to include contact elements or adjustment or assembly features for the next packaging steps.

For the MID body different plastic materials, such as PBT, PP and LCP can be used. To produce the 3D conductor tracks, three different processes are most commonly applied: LDS (Laser Direct Structuring), LSS (Laser Subtractive Structuring), and 2 shot molding.

In the LDS process, the conductor tracks are written by a laser onto the MID part, thereby activating a metal complex that is contained in the plastic material. These activated areas are subsequently metal plated in chemical solutions.

In the LSS process the entire surface is chemically activated and metallized. The structuring is carried out by means of laser ablation and/or exposure, with subsequent separation of the tracks in an etching process. Therefore, this represents a subtractive process.

The 2 shot mold is produced in a two-stage injection process, by injecting two different plastic components into the two molds to form the trace pattern on the surface. When using an “inert” plastic material and one with a good chemical metallization capability, the chemical plating process produces the trace pattern directly. Laser structuring of each element is therefore not needed.

The picture on page 16 of the previous article shows such an MID element in comparison with the size of a match.

It is produced with the LDS process and features various non-planar traces and electrical feedthroughs.

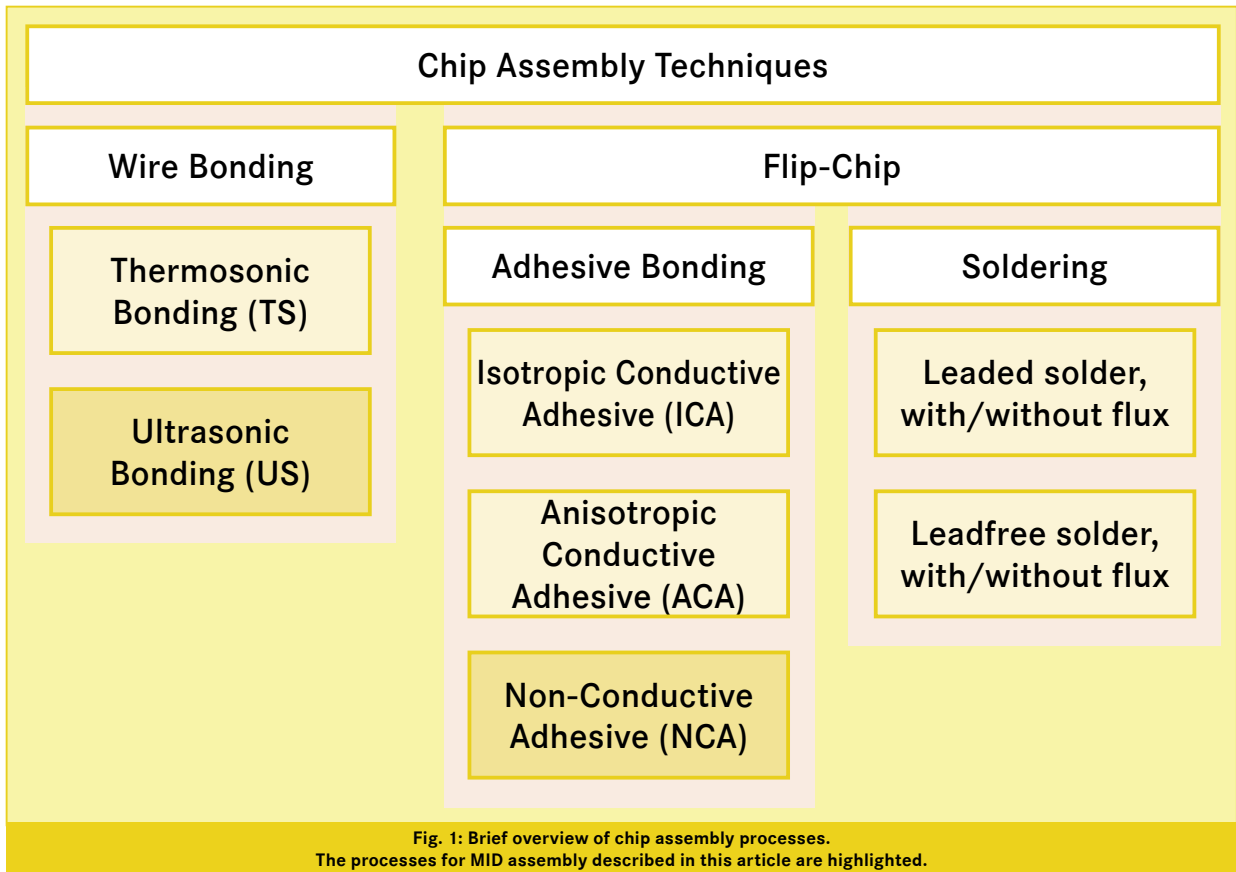
CHIP ASSEMBLY TECHNIQUES

A chip assembly consists of the mechanical and electrical connection of the basic unprotected Silicon (Si) chip to a housing or assembly substrate, including a first protection against various environmental influences. Original assembly techniques were primarily developed to assemble single chips in a stable package. The rising demand for higher package density has driven the development of several flip-chip assembly techniques. Fig. 1 provides a brief overview of the state-of-the-art chip assembly techniques.

The main differences of flip chip assemblies compared to wire bonded elements are found in spatial requirements, production processes and reliability requirements. Wire bonding needs a lot of space as the wires are fixed outside the chip and all together is covered by the Glob Top. It is a serial connection process and shows good stability because of the “flexible” electrical connections. The main advantages of flipchip processes are space savings and parallel bonding of all connections in a single step.

HARTING currently develops and deploys the two MID chip assembly techniques highlighted in Fig. 1. that will be described in the following. Wire bonding on planar substrates represents a commonly accepted technique, offering advantages such as a high degree of flexibility with respect to chip selection as all are wire bondable without auxiliary processes, and a higher degree of flexibility in the substrate layout due to the variable positions and lengths of the wire connections. The main reason of using an adhesive bonding process for flip-chip is due to the fact that the assembled MID modules itself are often subsequently soldered in a leadfree process, and any higher soldering temperatures to realize a solder hierarchy on the MID are excluded in view of the temperature limits of the plastic materials used.





WIRE BONDING

In the wire bonding process, the metal pads of the chip glued to the substrate are connected to the conductor tracks on the substrate using ultra-fine metal wires (usually Au or Al with a diameter of 25 µm to 70 µm). Those connections are made by locally welding the wire to the underlying metallization. The energy required in this process is provided by ultrasonic oscillation of the bonding tool (US process), or with additional heating (TS process.) Al wire bonding is carried out at room temperature. In contrast, the fact that Au wire bonding requires temperatures above 100 °C makes its application on plastic substrates more difficult, due to the poor heat conductive properties and tendency of deformation of the plastic materials under higher temperatures.

The transfer of this established wire bonding process on planar substrates to MID elements shows two critical aspects. A reasonable bonding capability requires a good transmission of the ultrasonic energy and fairly smooth metal layers.

A good energy transmission requires a ‘hard’ support of the bonding tool. On one hand, it needs a stable fixation of the component, which may require a highly complex clamp mechanism to secure the usually small MID components. Moreover, the component itself must provide an adequate inherent stiffness which is influenced by the plastic used, and by the layout and the metallization. The need of smooth metal surfaces conflicts with the requirements of adhesive strength of the metal layer on the plastic surface, as a certain roughness is prerequisite for

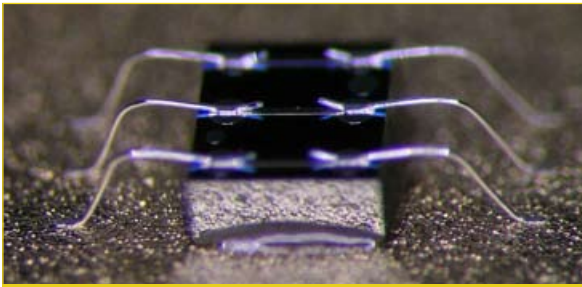


Fig. 2: Test chip, bonded with 33 μm Al wire on a metallized MID substrate

satisfactory adhesive strength. The various metallization processes produce surfaces with a different roughness. Although it is currently hardly feasible to bond LDS layers in an industrial process, the variation of laser parameters and of metal plating processes produce substantial improvements. In the 2 shot molding and LSS process, the corresponding plastic material is activated and metallized in a chemical process and thus allowing the production of bondable layers of sufficient smoothness. Fig. 2 shows a test chip which is glued to an MID substrate with such a metallization, and then wire bonded with a US process using Al wire of 33 μm diameter.

The use of injection molded elements as assembly substrates for wire bonding also offers specific advantages, as shown for example in Fig. 3. It is quite easy to produce assembly cavities in the mold to protect the chips mechanically and enable a simple and space saving application of the Glob Top. On planar substrates this

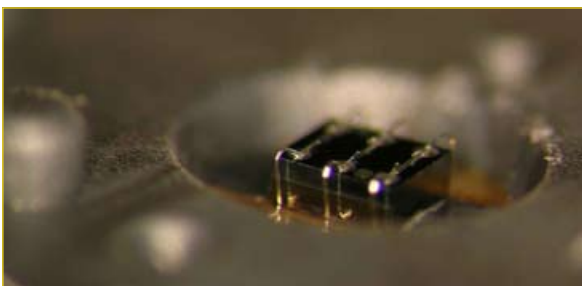


Fig. 3: Wire bonded chip in the cavity of a molded element, with alignment features (pin on the left) for further assembly processes

usually requires a dual-step process in which the chip is surrounded first by a dam which prevents wider distribution of the Glob Top applied on the chip and wires. The Glob Top is an encapsulant to protect and stabilize chip and bond wires.

NCA FLIP-CHIP

In Flip-Chip techniques, the chip is turned over, and the electrical chip pads are connected directly to the geometrically corresponding tracks on the substrate. Therefore, the chip has to be mechanically fixed in the same area as the electrical connections are carried out. In most processes (soldering and ICA = Isotropic Conductive Adhesive), this is done in two separate steps. In the first step, the electrical connections are produced by applying small dots of solder or conductive adhesive paste, that are fixed after assembly by soldering or curing. Next, an underfill is applied to protect the chip and its connections, as well as to provide adequate mechanical stability. The ACA (= Anisotropic Conductive Adhesive) and NCA (= Non-Conductive Adhesive) processes merge those two steps. These methods require electrically conductive bumps on the chip pads and/or tracks in order to guarantee proper electrical contact. In the ACA process, the adhesive contains few conductive particles which lead to a conductive connection at the location where they are squeezed during the assembly process. NCA is a non-conductive electrical adhesive which is cured under pressure and heat to realize a direct mechanical

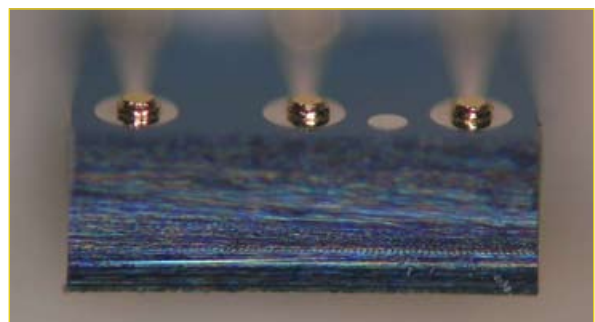


Fig. 4: Si test chip with Au stud bumps on the chip pads

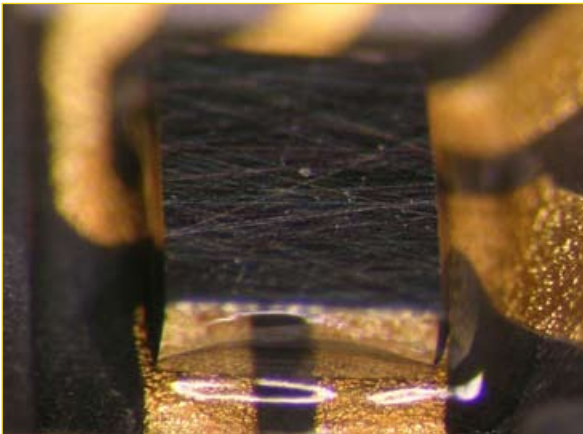


Fig. 5: NCA flip-chip assembled IC in an MID cavity with non-planar electrical lines

and electrical contact of the bumps to the metallized counterpart.

For the NCA Flip-Chip assembly on the MID substrates, the chips used are equipped with what is known as Au stud bumps. The latter are created in a standard Au ball bonding process, by immediately cutting of the wire after the first bond, and a levelling to the same height in a second step. Fig. 4 shows a side view of a test chip equipped with such Au stud bumps.

On the flip-chip substrate the electrical lines are routed underneath the chip to the connecting pads. On MIDs, these tracks can also be routed into cavities or around corners, thus allowing recessed assemblies and 3D arrangements. Fig. 5 shows an example of such a Flip-Chip assembly with the chip recessed in a cavity and connected electrically via the side walls.

The NCA assembly process offers the advantages of a single step process: electrical connections, fixation and protection are achieved in a single process. After the adhesive is applied to the chip area, the turned over chip is pressed down until the stud bumps make electrical contact. The pressure is maintained while the adhesive is cured within 10 to 30 seconds at a temperature between 150 °C and 200 °C. The shrinkage of the glue during curing guarantees for a reliable electrical and mechanical connection of the chip. Thereby, the chip sur-

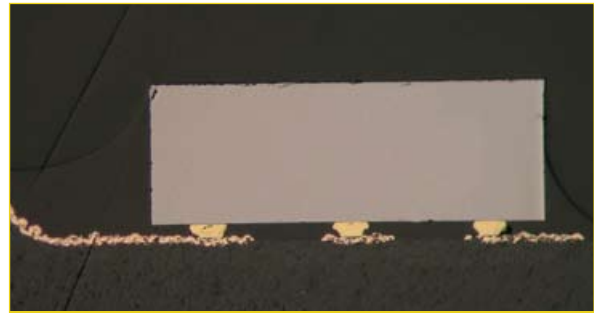


Fig. 6: Cross-section of a Flip-Chip assembly in MID cavity with electrical lines

face already facing down is also encapsulated and thus protected. Fig. 6 shows a polished cross-section of such a chip assembled in a cavity. The Au stud bumps on the chip pads are pressed onto the MID tracks produced by an LDS process, and are fixed alongside with the chip by the adhesive.

SUMMARY

In recent years, MID technology for the production of non-planar component carriers, with almost any shape of electrical lines, has established itself in many fields of sensor applications. New techniques for direct bare chip assembly on MID substrates contribute to a further expansion of this new technology. Sensors can be placed into a space-saving assembly, and often closer to the measuring point, while the density of chips in a 3D package can be increased even further. With the current expansion of the processes for chip assembly on MID substrates, HARTING is rounding off the entire MID process, from design to the end product.



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